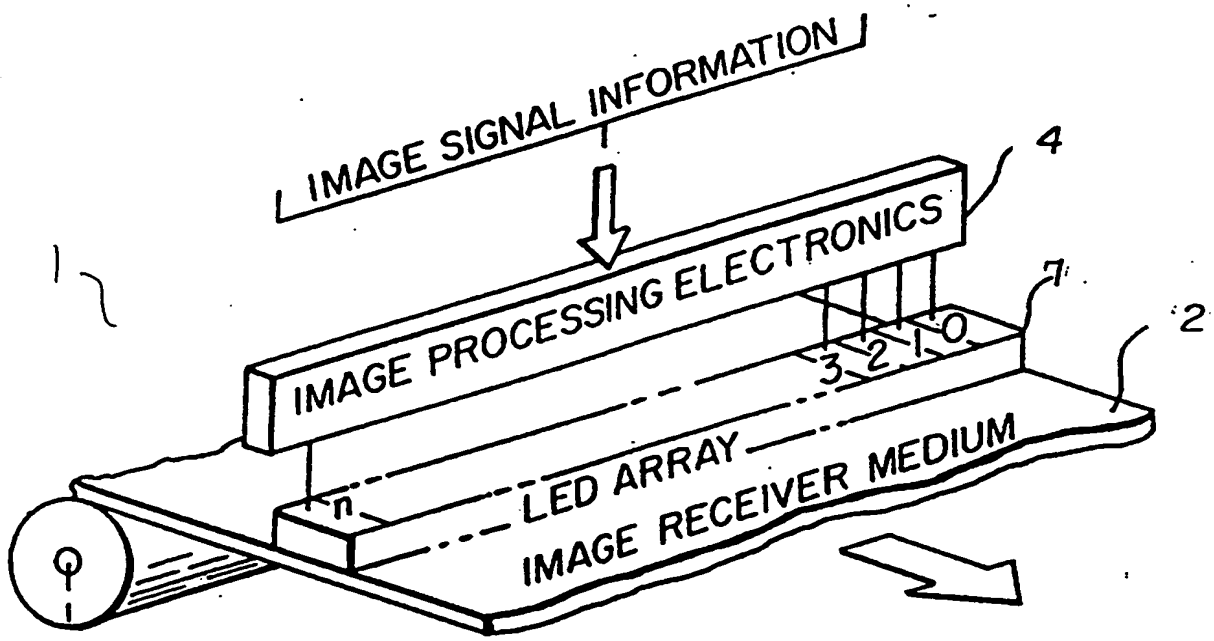


FIG. 1
PRIOR ART

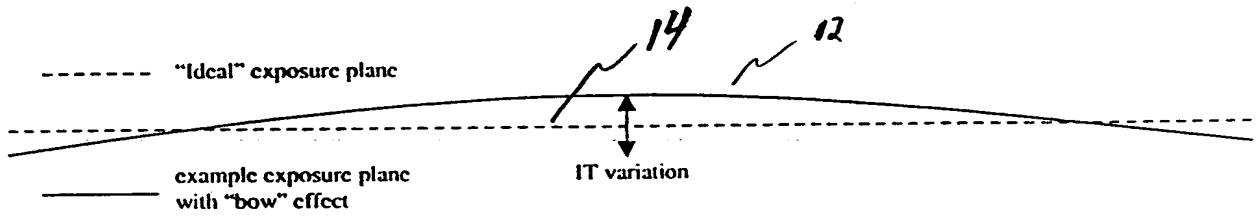


Figure 2a

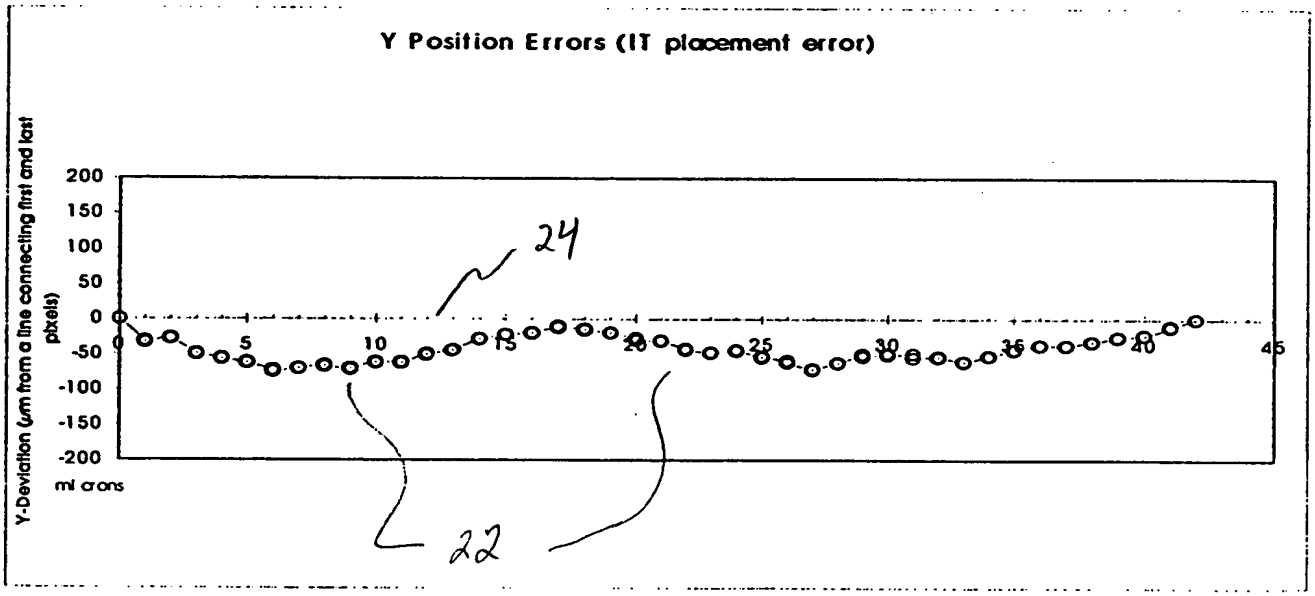


Figure 2b

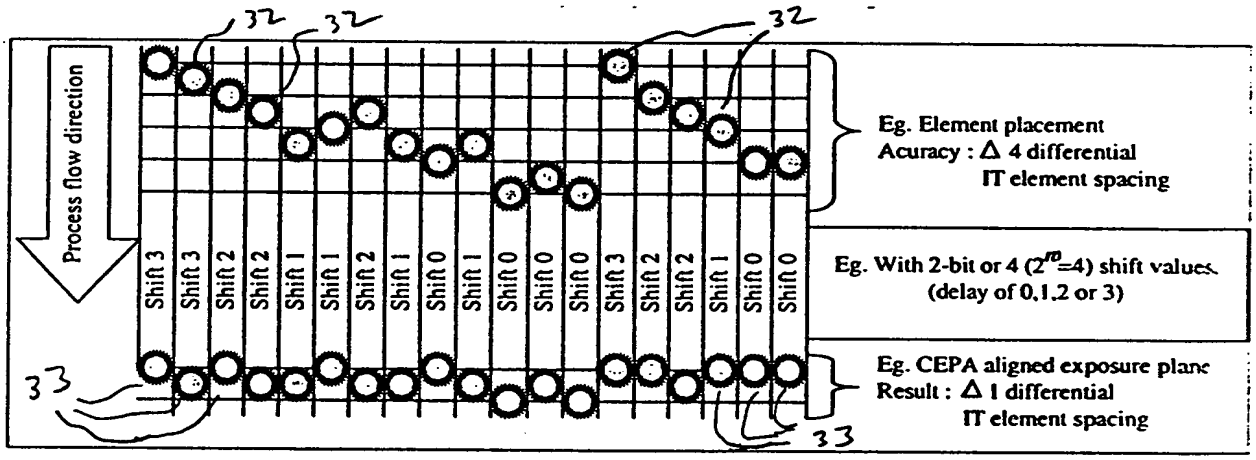


Figure 3 CEPA alignment example

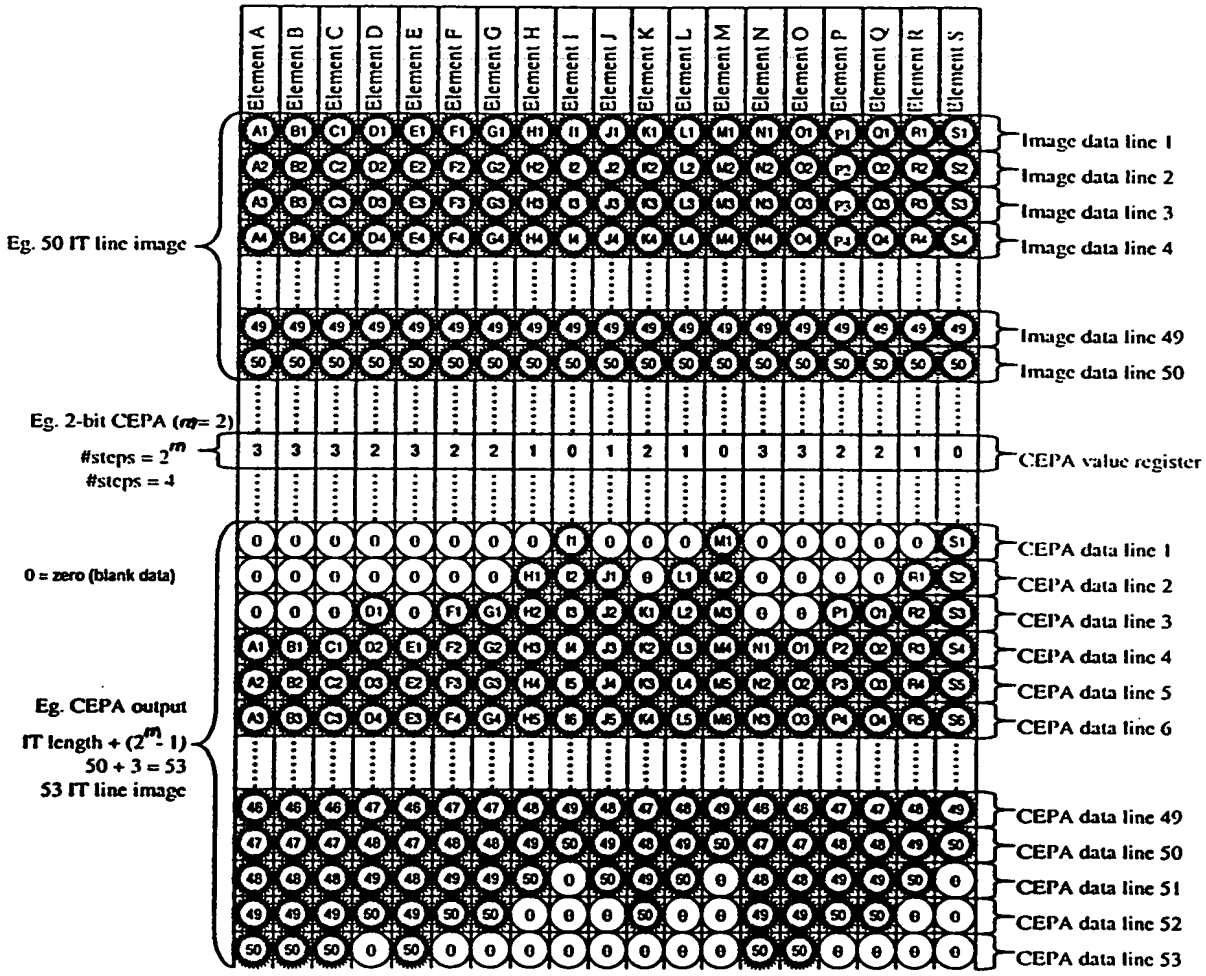


Figure 4 - CEPA data flow diagram

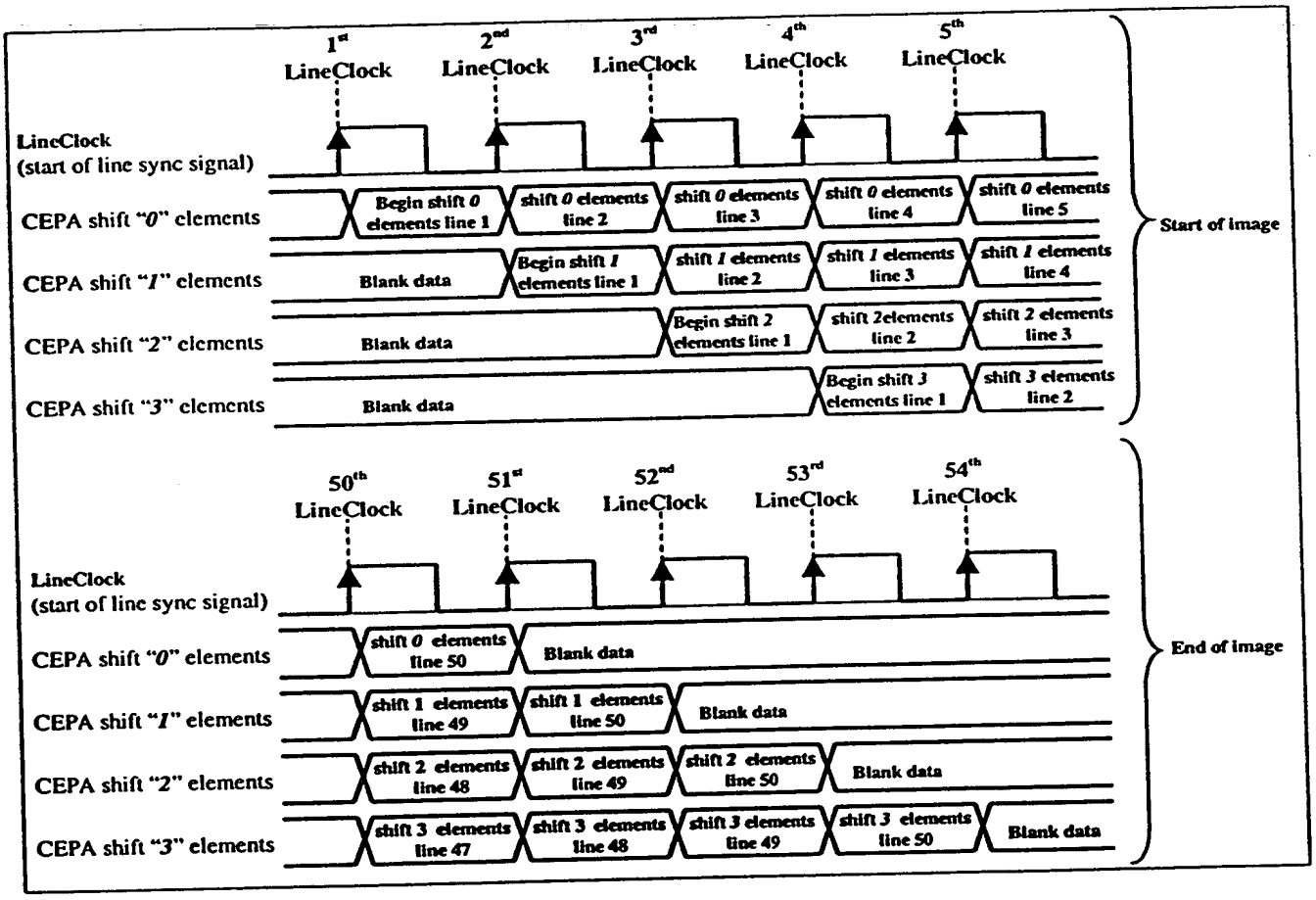


Figure 5 CEPA timing diagram (e.g. 50 IT line image)

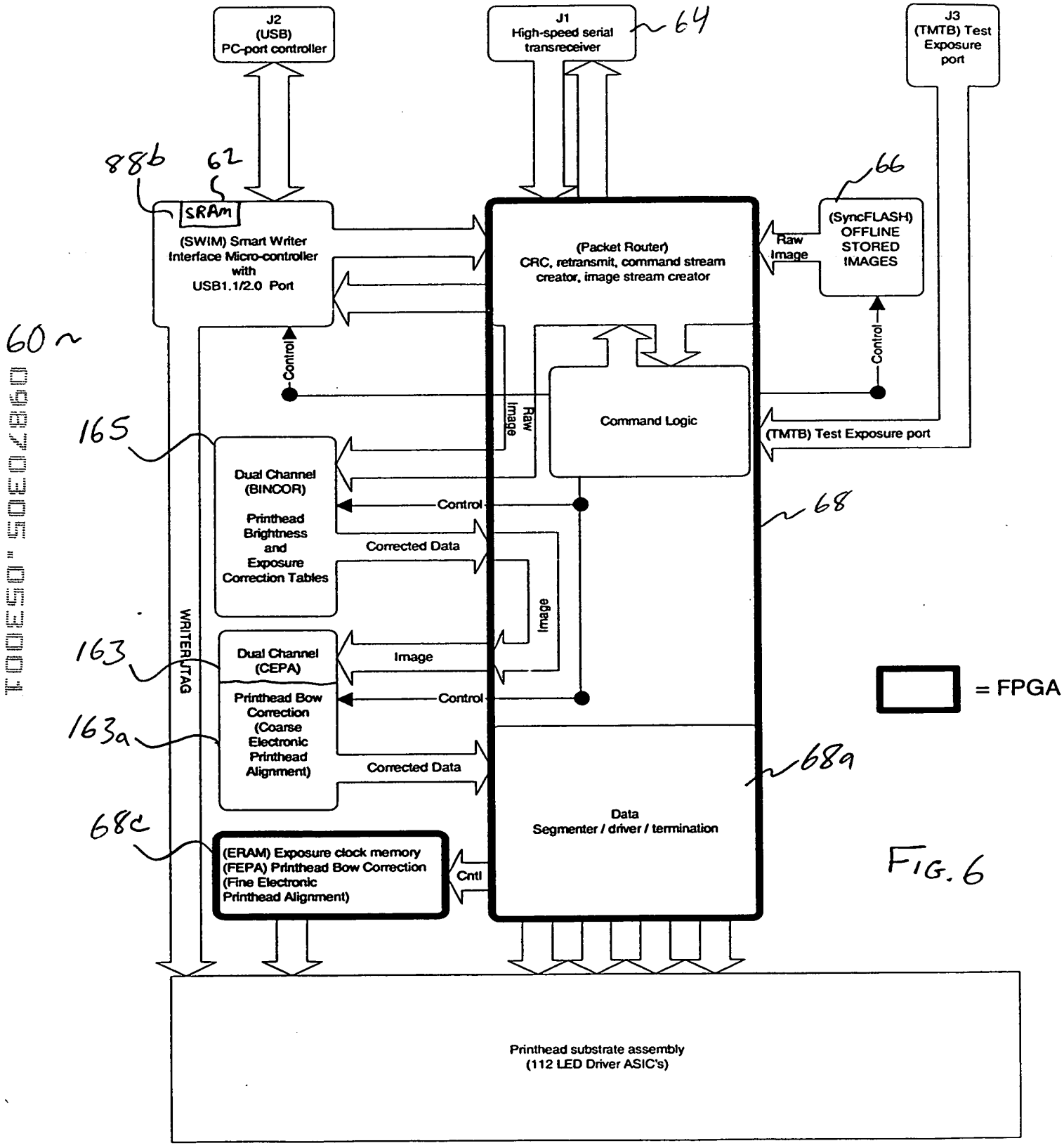

J2
(USB)
PC-port controller
J1
High-speed serial transreceiver
64
J3
(TMTB) Test Exposure port
86
62
SRAm
(SWIM) Smart Writer Interface Micro-controller with USB1.1/2.0 Port
(Packet Router)
CRC, retransmit, command stream creator, image stream creator
66
(SyncFLASH) OFFLINE STORED IMAGES
Raw Image
Control
Command Logic
(TMTB) Test Exposure port
60
165
Dual Channel (BINCOR)
Printhead Brightness and Exposure Correction Tables
Control
Corrected Data
Raw Image
68
Image
163
Dual Channel (CEPA)
Printhead Bow Correction (Coarse Electronic Printhead Alignment)
Image
Control
Corrected Data
WRITER JTAG
= FPGA
163a
68a
Data
Segmenter / driver / termination
68c
(ERAM) Exposure clock memory
(FEPA) Printhead Bow Correction
(Fine Electronic Printhead Alignment)
Cntl
Printhead substrate assembly
(112 LED Driver ASIC's)

FIG. 6

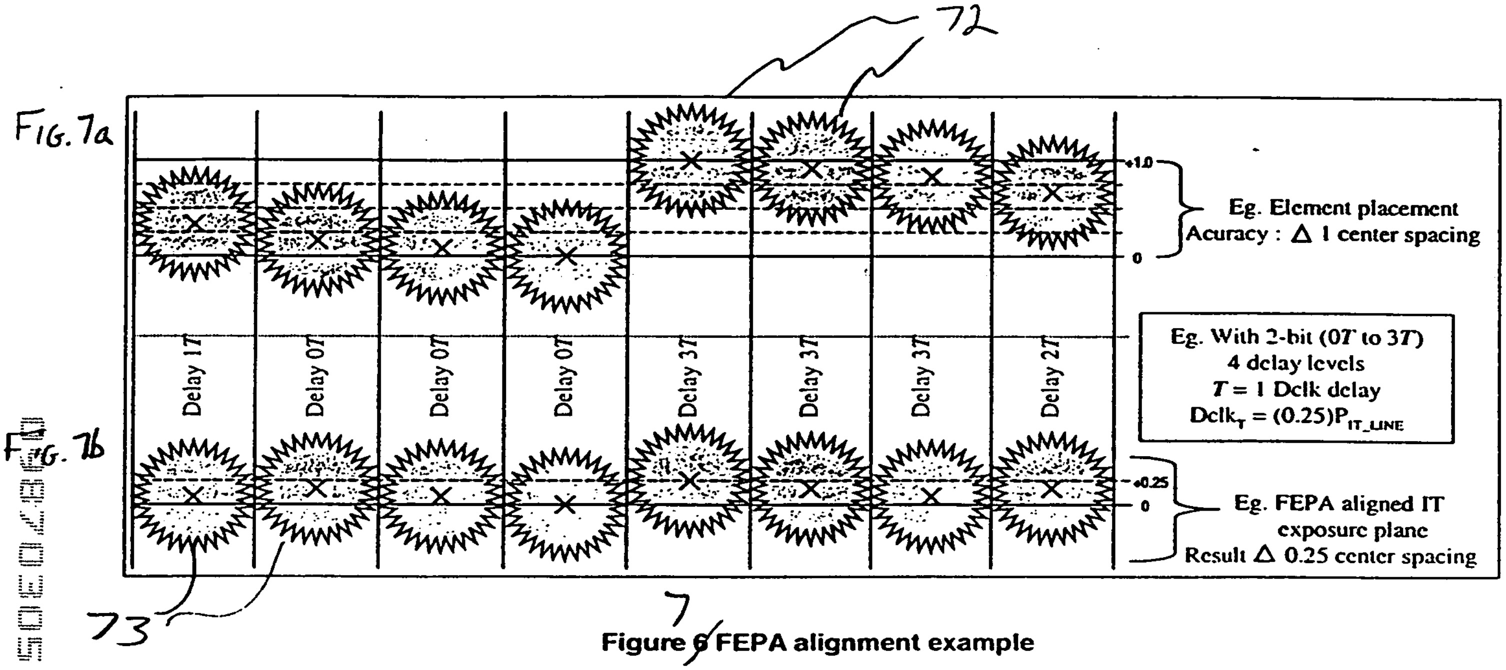


Figure 7 FEPA alignment example

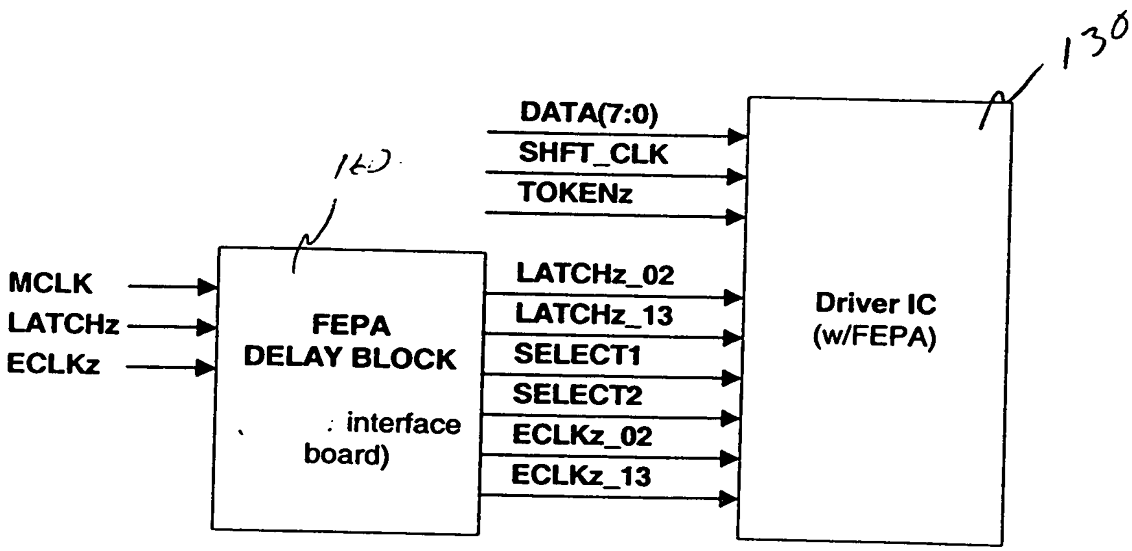


FIG. 8a FEPA BLOCK DIAGRAM

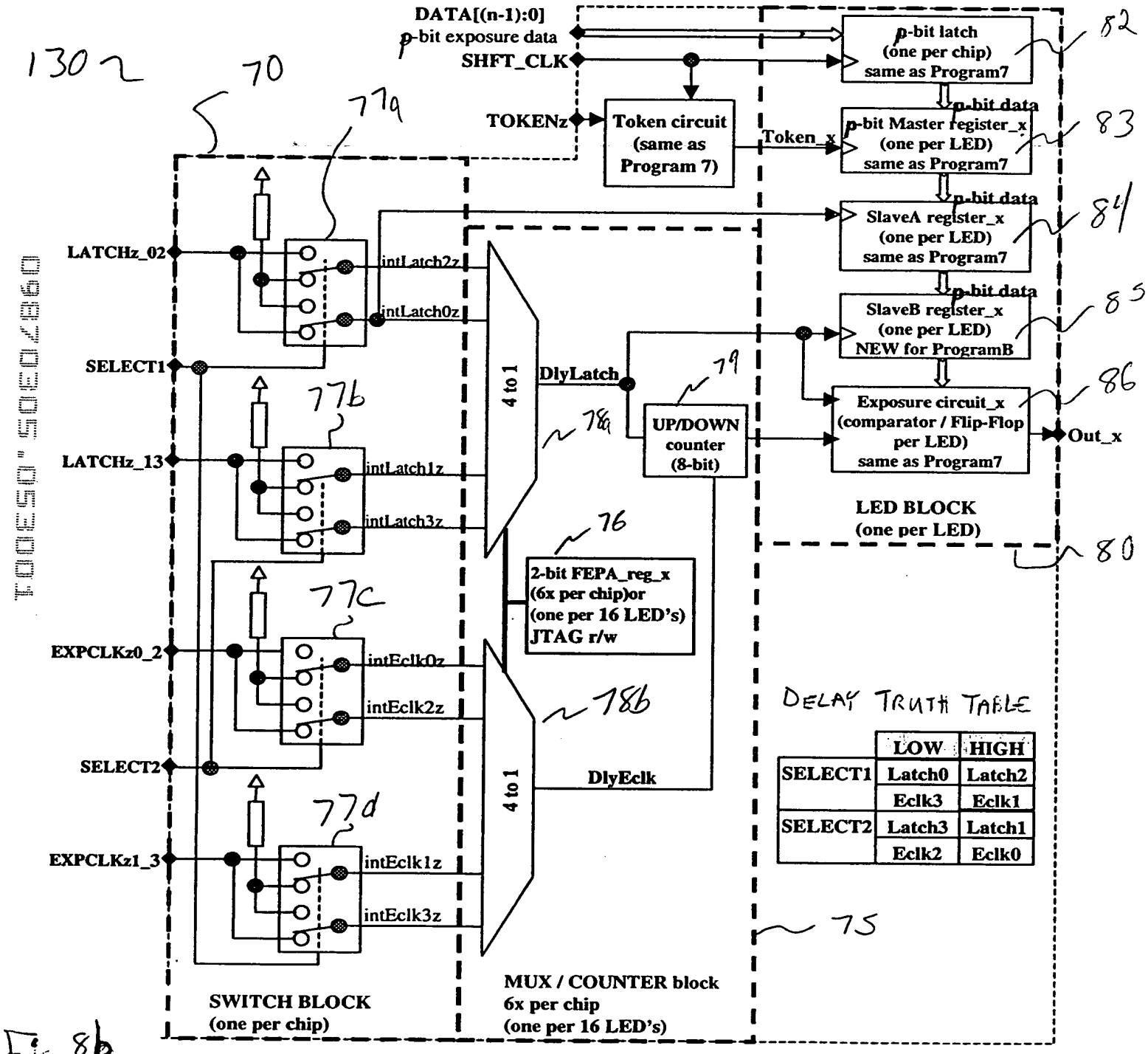

DATA[(n-1):0]
p-bit exposure data
SHFT_CLK
TOKENz
Token circuit (same as Program 7)
Token_x
p-bit latch (one per chip) same as Program7
p-bit Master register_x (one per LED) same as Program7
SlaveA register_x (one per LED) same as Program7
SlaveB register_x (one per LED) NEW for ProgramB
Exposure circuit_x (comparator / Flip-Flop per LED) same as Program7
Out_x
p-bit data
LED BLOCK (one per LED)
LATCHz_02
LATCHz_13
EXPCLKz0_2
EXPCLKz1_3
SELECT1
SELECT2
intLatch2z
intLatch0z
intLatch1z
intLatch3z
intEclk0z
intEclk2z
intEclk1z
intEclk3z
4 to 1
DlyLatch
DlyEclk
UP/DOWN counter (8-bit)
2-bit FEPA_reg_x (6x per chip)or (one per 16 LED's) JTAG r/w
SWITCH BLOCK (one per chip)
MUX / COUNTER block 6x per chip (one per 16 LED's)
DELAY TRUTH TABLE
LOW
HIGH
SELECT1
Latch0
Latch2
Eclk3
Eclk1
SELECT2
Latch3
Latch1
Eclk2
Eclk0
1302
70
77a
77b
77c
77d
78a
78b
79
75
76
80
82
83
84
85
86

Fig 8b

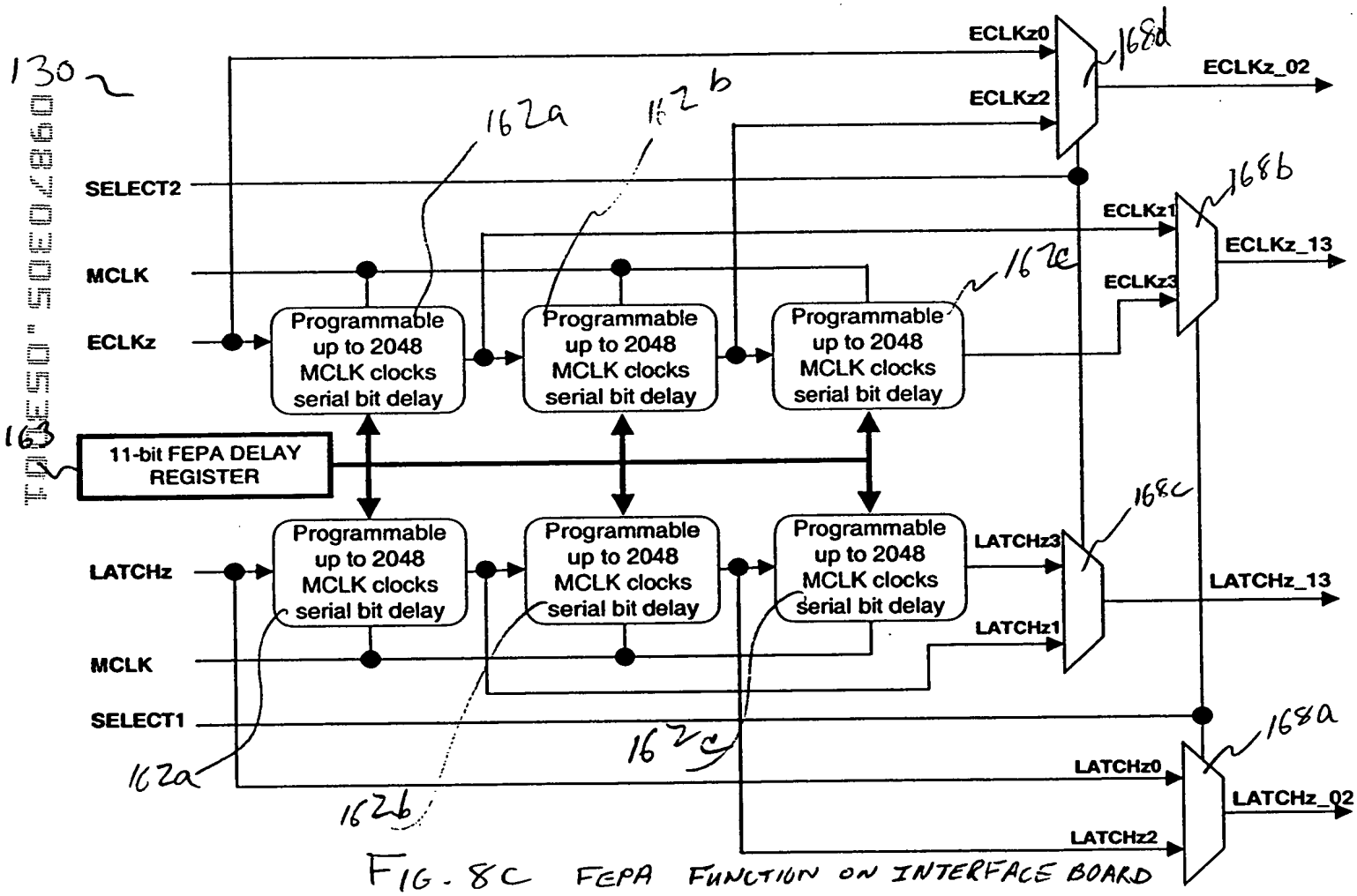


FIG. 8C FEPA FUNCTION ON INTERFACE BOARD

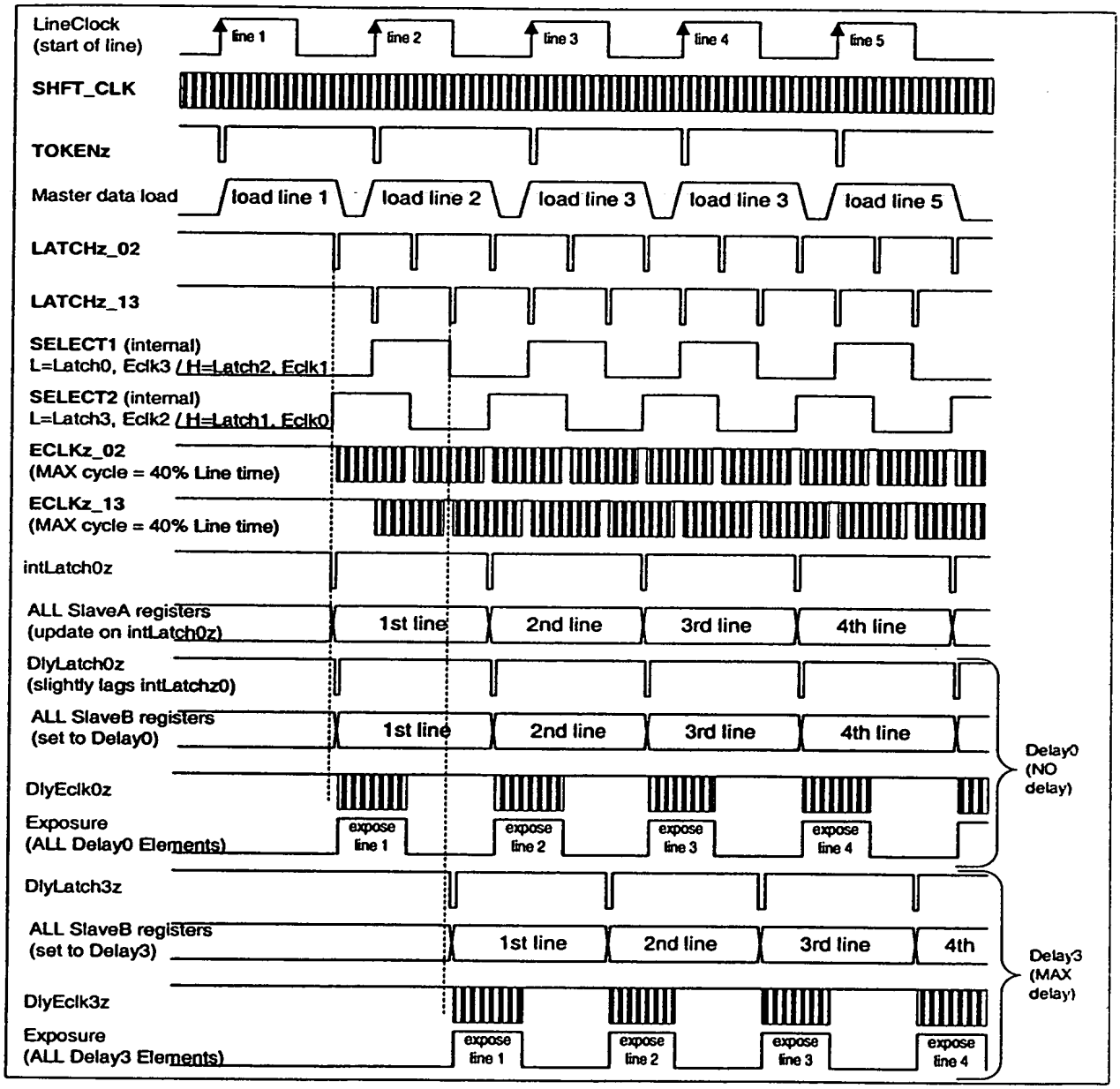

LineClock
(start of line)
line 1
line 2
line 3
line 4
line 5
SHFT_CLK
TOKENz
Master data load
load line 1
load line 2
load line 3
load line 3
load line 5
LATCHz_02
LATCHz_13
SELECT1 (internal)
L=Latch0, Eclk3 / H=Latch2, Eclk1
SELECT2 (internal)
L=Latch3, Eclk2 / H=Latch1, Eclk0
ECLKz_02
(MAX cycle = 40% Line time)
ECLKz_13
(MAX cycle = 40% Line time)
intLatch0z
ALL SlaveA registers
(update on intLatch0z)
1st line
2nd line
3rd line
4th line
DlyLatch0z
(slightly lags intLatchz0)
ALL SlaveB registers
(set to Delay0)
1st line
2nd line
3rd line
4th line
DlyEclk0z
Exposure
(ALL Delay0 Elements)
expose line 1
expose line 2
expose line 3
expose line 4
Delay0
(NO delay)
DlyLatch3z
ALL SlaveB registers
(set to Delay3)
1st line
2nd line
3rd line
4th
DlyEclk3z
Exposure
(ALL Delay3 Elements)
expose line 1
expose line 2
expose line 3
expose line 4
Delay3
(MAX delay)

Fig 8d

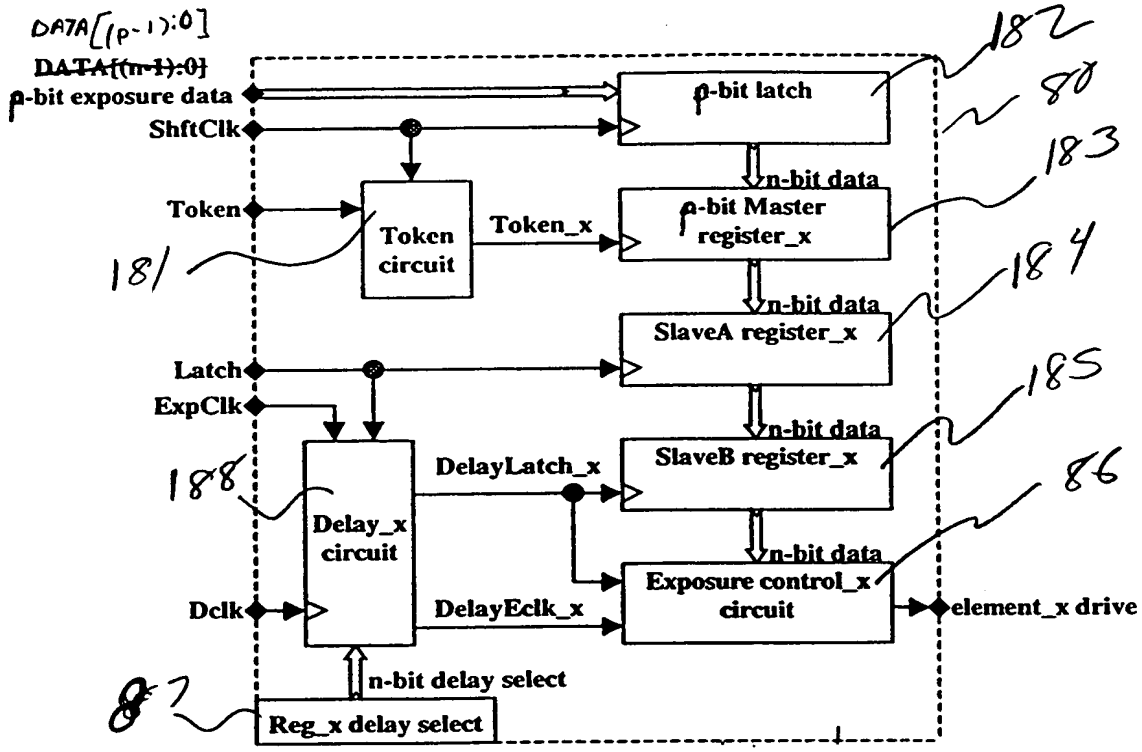


FIG. 9A FEPA DIAGRAM for Second Preferred Embodiment
Block

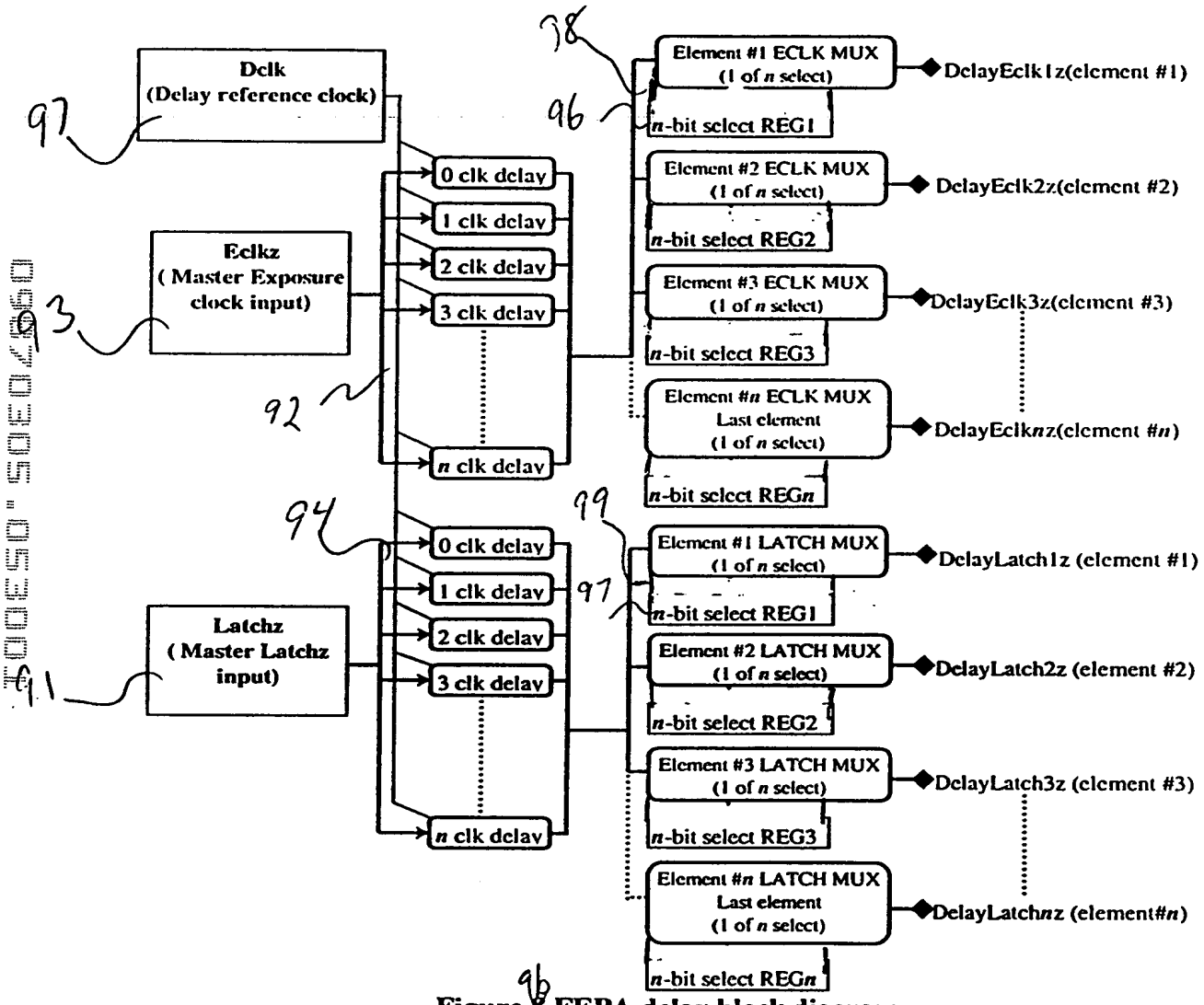
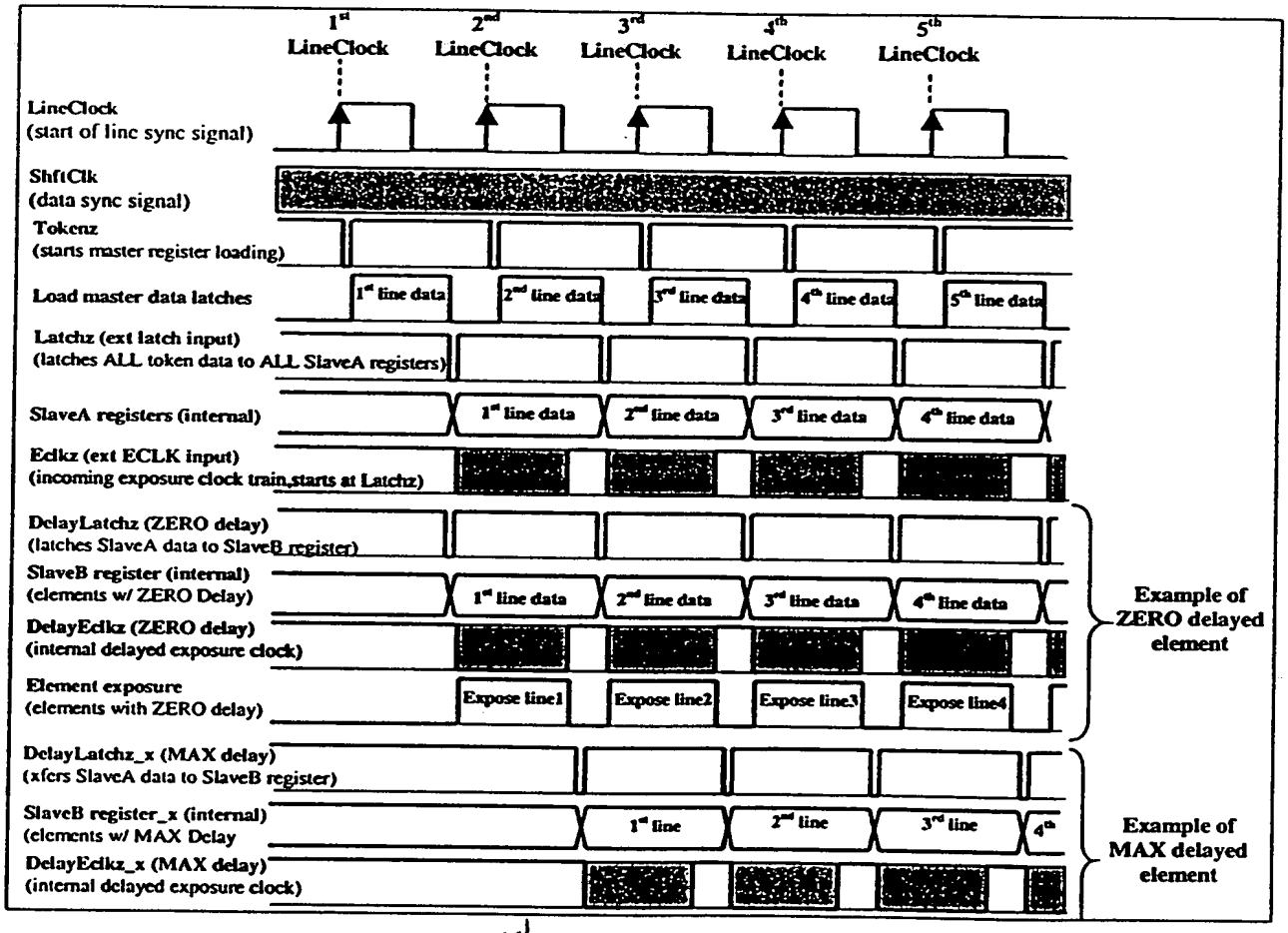


Figure 8 FEPA delay block diagram



10

Figure 9 FEPA signal timing diagram

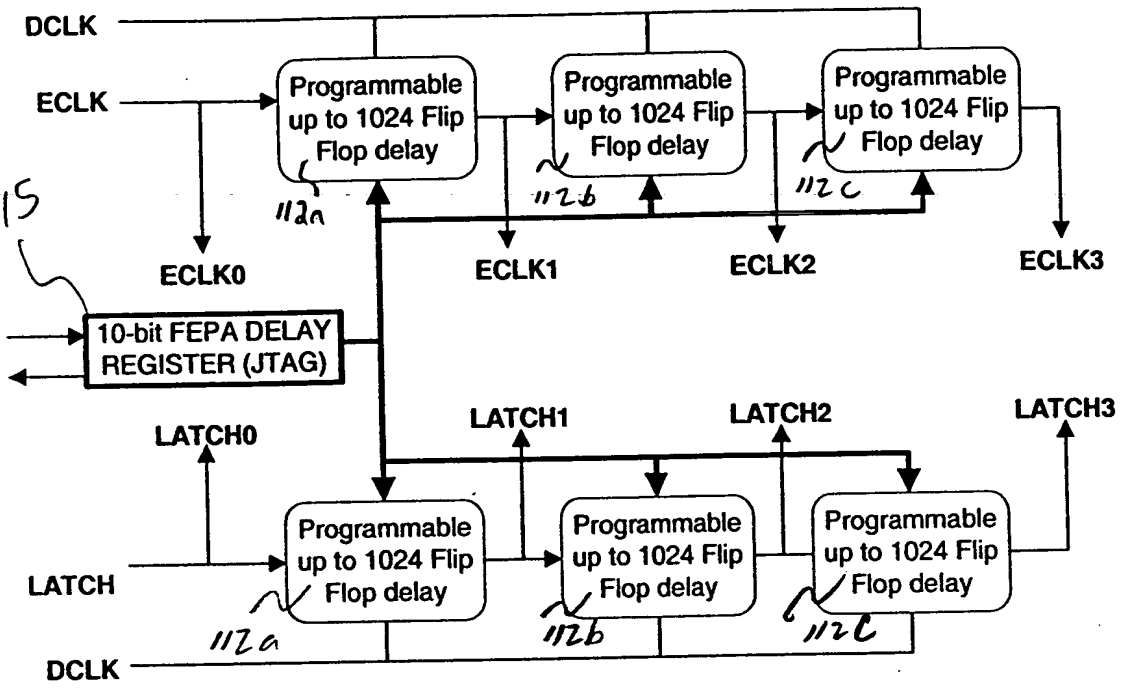


FIG. 11

FEPA DELAY CIRCUIT (ONE PER DRIVER IC)

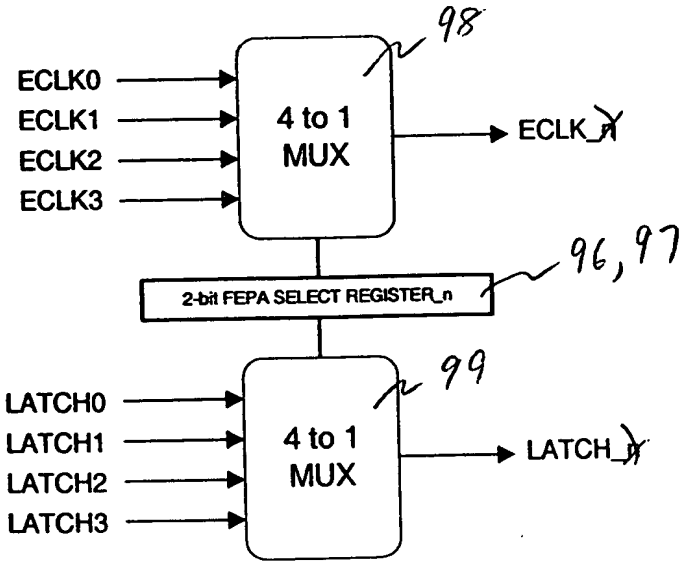


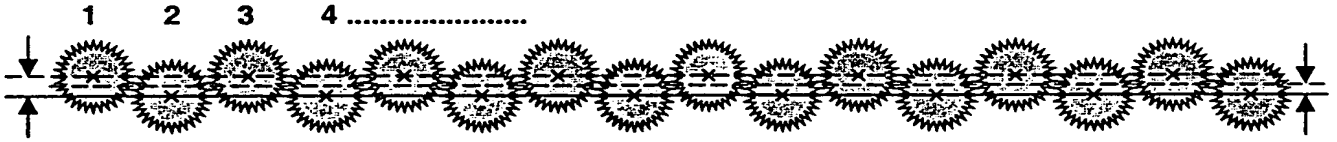
FIG. 12

FEPA DELAY SELECT CIRCUIT (ONE PER LED)

FIG 13a

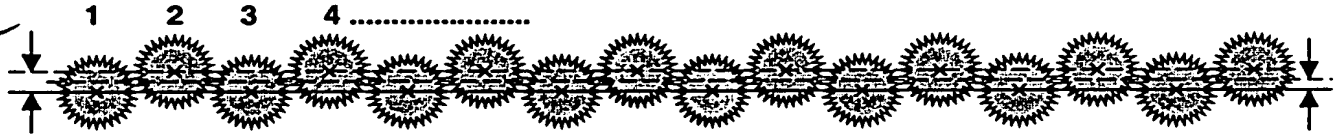
Odd and even shifted same

FIG 13b



Odd's only shifted +1/4 delta producing +1/8 average shift appearance

FIG 13c



Even's only shifted +1/4 producing +1/8 average average shift appearance

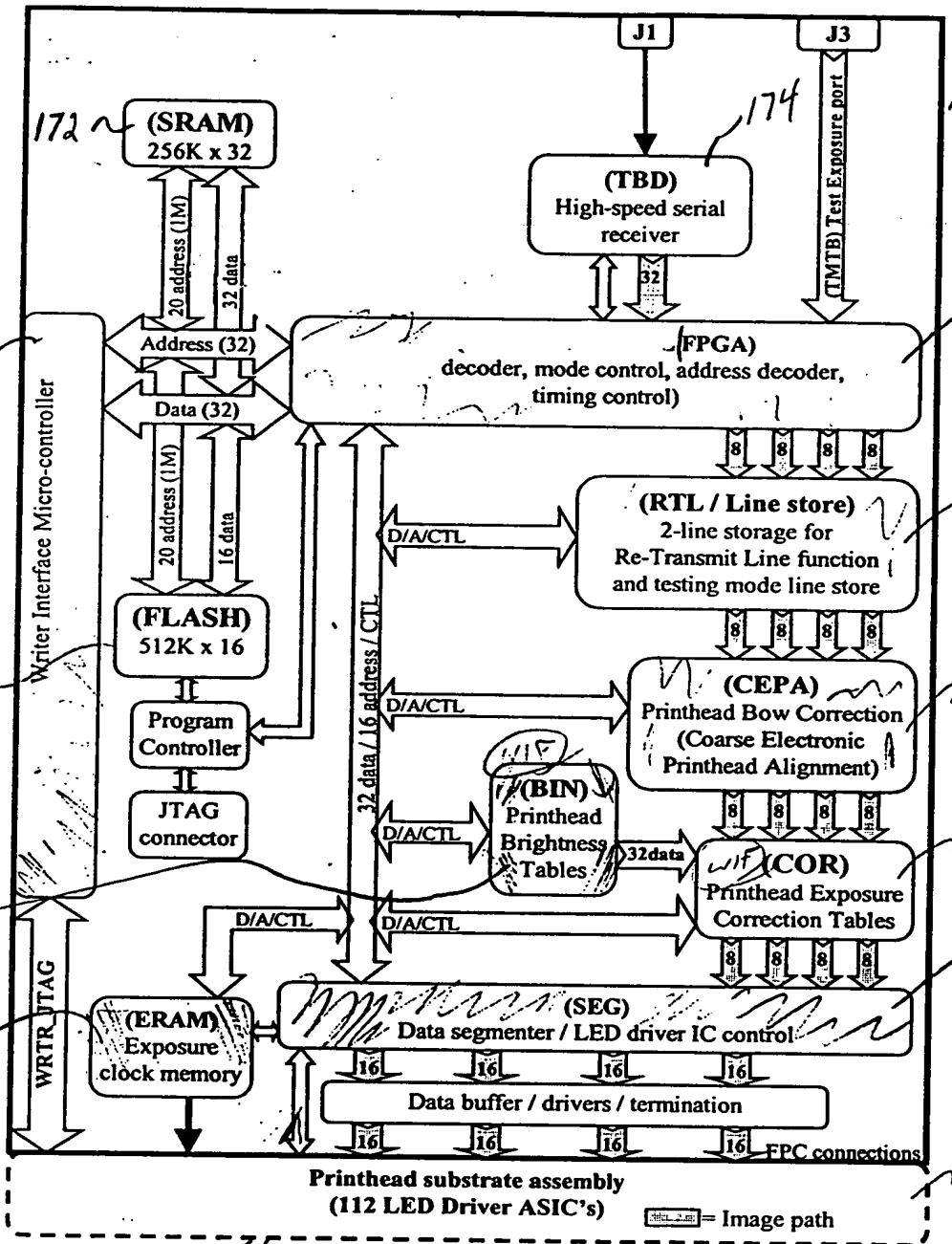


Figure 14 ~~SWIFT~~ board block diagram (FPGA function's shaded)

Interface

Fig. 14